WHAT IS CLAIMED IS:

1. A method for fabricating a low temperature polysilicon thin film transistor, comprising:

providing a substrate;

forming a polysilicon layer on the substrate;

forming a gate oxide layer on the polysilicon layer;

forming a photoresist pattern on the gate oxide layer;

etching the polysilicon layer and the gate oxide layer using the photoresist pattern as a mask;

removing the photoresist pattern;

forming a gate on the gate oxide layer; and

implanting dopants to form a source/drain region using the gate as a mask.

2. The method according to claim 1, further comprising forming a buffer layer on the substrate prior to forming the polysilicon layer on the substrate.

3. The method according to claim 1, wherein the polysilicon layer has a thickness between about 200 angstroms and 1000 angstroms.

4. The method according to claim 1, wherein the gate oxide layer has a thickness between about 500 angstroms and 1500 angstroms.

5. The method according to claim 1, wherein the gate comprises molybdenum (Mo), chromium (Cr), thallium/aluminum/thallium (Ti/Al/Ti), or a combination thereof.

6. The method according to claim 1, wherein the dosage of the dopants implanted is between about 1E14dose/cm^2 and 5E15dose/cm^2.

7. A method for fabricating a first type transistor and a second type transistor on a substrate, comprising:

forming a polysilicon layer on the substrate;

forming a gate oxide layer on the polysilicon layer;

forming a photoresist pattern on the gate oxide layer;

etching the polysilicon layer and the gate oxide layer to form a first stack structure corresponding to the first type transistor and a second stack

structure corresponding to the second type transistor using the photoresist pattern as a mask;

removing the photoresist pattern;

forming a gate, occupying a smaller region than the gate oxide layer, on the gate oxide layer;

forming a source/drain region by implanting first heavy dopants in the first type transistor beside the gate and using a photoresist layer covering the second stack structure and a lightly doped region of the first type transistor as a mask;

implanting first dopants in the first type transistor to form the lightly doped region using the gate as a mask; and

forming a source/drain region of the second type transistor by implanting second heavy dopants using a photoresist layer over the first stack structure as a mask.

8. The method according to claim 7, further comprising forming a buffer layer on the substrate prior to forming the polysilicon layer on the substrate.

9. The method according to claim 7, after forming the source/drain region

of the second type transistor, further comprising:

forming an interlayer dielectric on the gate oxide layer, the gate and the substrate;

selectively exposing the gates, the source/drain regions of the first type transistor and the second type transistor; and

forming electrodes to electrically connect the gate and the source/drain region of the first type transistor and electrically connect the gate and the source/drain region of the second type transistor, respectively.

10. The method according to claim 9, wherein the interlayer dielectric has a thickness between about 2000 angstroms and 7000 angstroms.

11. The method according to claim 9, wherein the gate comprises molybdenum (Mo), chromium (Cr), thallium/aluminum/thallium (Ti/Al/Ti), or a combination therof.

12. The method according to claim 9, after forming the electrodes, further comprising:

forming a patterned passivation layer on the interlayer dielectric and the electrodes, wherein the patterned passivation layer exposes a portion of

the electrode of the first type transistor located within a pixel area; and

forming a transparent electrode to electrically connect the exposed portion of the electrode of the first type transistor.

13. The method according to claim 12, wherein the transparent electrode comprises indium tin oxide (ITO).

14. The method according to claim 7, wherein the polysilicon layer has a thickness between about 200 angstroms and 1000 angstroms.

15. The method according to claim 7, wherein the gate oxide layer has a thickness between about 500 angstroms and 1500 angstroms.

16. The method according to claim 7, wherein the gate comprises molybdenum (Mo), chromium (Cr), thallium/aluminum/thallium (Ti/Al/Ti), or a combination thereof.

17. The method according to claim 7, wherein the dosage of the first heavy dopants is between about 1E14 dose/cm^2 and 5E15 dose/cm^2.

18. The method according to claim 7, wherein the dosage of the first light dopants implanted is between about 8E12 dose/cm^2 and 5E13 dose/cm^2.

19. The method according to claim 7, wherein the dosage of the second heavy dopants implanted is between about 1E14 dose/cm^2 and 5E15 dose/cm^2.

20. The method according to claim 7, wherein the first type transistor is a NMOS transistor and the second type transistor is a PMOS transistor.

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